Docket No.: 004192.P053D B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:	)	
	)	Examiner: Kang, Donghee
Min-hwa Chi	)	
	)	Art Group: 2811
Application No.: 09/865,929	)	
	)	
Filed: May 24, 2001	)	
	)	
For: TRANSISTOR AND LOGIC CIRCUIT ON THIN SILICON-ON-INSULATOR WAFERS BASED ON GATE INDUCED DRAIN LEAKAGE CURRENTS	)	

Mail Stop: Issue Fee (Drawings)
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF FORMAL DRAWINGS

Dear Sir/Madam:

Enclosed herewith for filing in the above-identified U.S. patent application are the formal drawings, Figures 1-12 (9 sheets).

Respectfully submitted,
BLAKELY SOKOLOFF TAYLOR & ZAFMAN, LLP

Date: 8/12/03

Jan Carol Little
Reg. No. 41,181

Certificate of Mailing:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Mail Stop: Issue Fee (Drawings), Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

on August 12, 2003
Date of Deposit

Luci M. Arevalo
Name of Person Mailing Correspondence

Signature

August 12, 2003
Date